IN THE CLAIMS

Please amend the claims as follows:

Claims 1-6 (Canceled).

Claim 7 (Currently Amended): An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof;

a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate and each recessed at a first distance (L5) and a second distance (L6) alternately, lower ends of said trenches extending to a predetermined depth ~~extending~~ from the surface of said semiconductor substrate to an upper portion of said N-type base layer;

a gate ~~oxide layer~~ insulating film provided on an inner surface of each of said trenches and on the surface of said semiconductor substrate;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate ~~oxide layer~~ insulating film and connected to said gate wire, with one set of said trench gate electrodes being constituted by ~~twos~~ two arranged in sequence at the first distance (L5), and said first distance (L5) is greater than said second distance (L6);

an N-type emitter layer provided in the surface part of said P-type base layer having a length of said second distance (L6) interposed between said trench gate electrode belonging to said one set of electrodes and said trench gate electrodes belonging to another set of electrodes adjacent to said one set of electrodes, and in the vicinity of said trench gate electrode;

an insulating ~~oxide~~ layer provided covering a part or the whole of said trench gate electrode, and holed with contact holes at each of portions provided with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating ~~oxide~~ layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on said P-type emitter layer on the underside of said semiconductor substrate;

wherein the predetermined depth of the trench is set to such an extent that a depletion layer formed extending from a ~~top~~ tip of said trench gate electrode at a voltage lower than that which generates breakdown when [[in]] a forward voltage ~~application is fused~~ is applied, fuses with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and such that a curvature of said depletion layer at the ~~top~~ tip of said trench gate electrode is relieved.

Claims 8-10 (Canceled).

Claim 11 (Previously Presented): An insulating gate type semiconductor device according to Claim 7, wherein the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3 μm or less.

Claim 12 (Currently Amended): An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof;

a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate, said plurality of trenches constituting a set of trenches, each set of trenches being disposed at an interval having a first distance (L5), each of said set of trenches having a second distance (L6) between both end trenches, and said first distance (L5) is greater than said second distance (L6);

an N-type emitter provided in the surface part of said P-type base layer having a width of the second distance;

a gate ~~oxide layer~~ insulating film provided at least on an inner surface of each of said trenches;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate ~~oxide layer~~ insulating film and connected to said gate wire;

an insulating ~~oxide~~ layer provided covering said trench gate electrode, and holed with contact holes at each of portions with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating ~~oxide~~ layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on the underside of said P-type emitter layer,

wherein lower ends of said trenches extending to a depth from the surface of said semiconductor substrate to an upper portion of said N-type base layer to such an extent that a depletion layer formed extending from a tip of said trench gate electrode at a voltage lower than that which generates breakdown when [[in]] a forward voltage ~~application is fused~~ is applied, fuses with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and such that a curvature of said depletion layer at the tip of said trench is relieved.

Claim 13 (Previously Presented): An insulating gate type semiconductor device according to claim 12, wherein the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3 μm or less.

Claim 14 (Currently Amended): An insulating gate type semiconductor device according to claim 12, wherein said insulating ~~oxide~~ layer is provided on the part or [[of]] whole surface of said trench gate electrodes on said P-type base layer between a set of trenches and a next set of trenches.

Claim 15 (New): An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and P-type base layers are formed in sequence from the underside thereof to the surface thereof;

a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate and each recessed at a first distance (L5) and a second distance (L6) alternately, lower ends of said trenches extending to a predetermined depth from the surface of said semiconductor substrate to an upper portion of said N-type base layer,

a gate insulating film provided on an inner surface of each of said trenches and on the surface of said semiconductor substrate;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate insulating film and connected to said gate wire, with one set of said trench gate electrodes being constituted by two arranged in sequence at the first distance (L5), and said first distance (L5) is greater than said second distance (L6);

a plurality of N-type emitter layers provided in the surface parts of said P-type base layers having a length of said second distance (L6) interposed between said trench gate electrode belonging to said one set of electrodes and said trench gate electrode belonging to another set of electrodes adjacent to said one set of electrodes and in the vicinity of said trench gate electrode;

an insulating oxide layer provided covering a part or the whole of said trench gate electrode, and holed with contact holes at each of portions provided with said P-type base layers and said N-type emitter layers;

an emitter electrode provided covering said insulating layer and connected commonly to said P-type base layers and said N-type emitter layers; and

a collector electrode provided on said P-type emitter layer on the underside of said semiconductor substrate,

wherein the predetermined depth of the trench is set to such an extent that a depletion layer formed extending from a tip of said trench gate electrode at a voltage lower than that which generates breakdown when a forward voltage is applied, fuses with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and such that a curvature of said depletion layer at the tip of said trench gate electrode is relieved.

Claim 16 (New): An insulating gate type semiconductor device according to claim 15, wherein the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3 μm or less.

Claim 17 (New): An insulating gate type semiconductor device comprising:

a semiconductor substrate on which a P-type emitter layer, an N-type base layer and a P-type base layer are formed in sequence from the underside thereof to the surface thereof;

a plurality of trenches arranged substantially in parallel throughout said semiconductor substrate, said plurality of trenches constituting set of trenches, each set of trenches being disposed at an interval having a first distance (L5), each of said set of trenches having a second distance (L6) between both end trenches, said first distance (L5) is greater than said second distance (L6);

an N-type emitter provided in the surface part of said P-type base layer having a width of the second distance;

a gate insulating film provided at least on an inner surface of each of said trenches;

a gate wire for transmitting a voltage applied to a gate;

a plurality of sets of trench gate electrodes each provided in said each trench formed with said gate insulating film and connected to said gate wire;

an insulating layer provided coveting said trench gate electrode, and holed with contact holes at each of portions with said P-type base layer and said N-type emitter layer;

an emitter electrode provided covering said insulating layer and connected to said P-type base layer and said N-type emitter layer; and

a collector electrode provided on the underside of said P-type emitter layer,

wherein lower ends of said trenches extending to a depth from the surface of said semiconductor substrate to an upper portion of said N-type base layer to such an extent that a depletion layer formed extending from a tip of said trench gate electrode at a voltage lower than that which generates breakdown when a forward voltage is applied, fuses with a depletion layer formed extending from a junction area between said N-type base layer and said P-type base layer to which said trench gate electrode is vicinal and such that a curvature of said depletion layer at the tip of said trench is relieved.

Claim 18 (New): An insulating gate type semiconductor device according to claim 17, wherein the predetermined depth of the trench is such a depth that a depth from the junction surface between said N-type base layer and said P-type base layer is 3 μm or less.

Claim 19 (New): An insulating gate type semiconductor device according to claim 17, wherein said insulating layer is provided on the part or whole surface of said trench gate electrodes on said P-type base layer between a set of trenches and a next set of trenches.